ABSTRACT

The present invention includes a semiconductor package that forms the solder array joints on the die surface and corresponding BGA substrate and PCB respectively. The life times of array solder joints are increased through the use of two sets of array joints. The top array comprises a plurality of high melting solder joints and a plurality of low melting solder joints, while the bottom array comprises a plurality of high melting solder joints only. The reflow temperature of SMT assembly is between the aforementioned high melting point and low melting point of solder joints. In addition, each solder joint comprises a flat surface at its front edge.